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SMALL-SIGNAL ANALYSIS OF A PWM BOOST DC-DC CONVERTER WITH A NON-SYMMETRIC PHASE INTEGRAL-LEAD CONTROLLER

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Abstract - An extensive small-signal analysis of a single-loop voltage-mode-control strategy for a pulse-width-modulated (PWM) boost DC-DC power converter operating in continuous conduction mode (CCM) is proposed using a new non-symmetric phase controller. To model the boost power stage, a linear circuit model is used which includes all parasitic components such as the equivalent series resistance (ESR) of the filter capacitor, the ESR of the inductor, the transistor ON-resistance, and the diode forward resistance and offset voltage. The proposed control scheme introduces a new non-symmetric phase integral-lead controller. The controller can provide a peak phase boost of up to 165° , with its phase returning to 0° at high frequencies. This phase characteristic is much improved over that of a commonly used symmetric phase integral-lead controller which provides -90° of phase at high frequencies. The new controller characteristics provide increased gain margin and phase margin for a DC-DC converter. Open-loop and closed-loop circuit models and transfer functions are derived for the boost PWM converter and illustrated by Bode plots.

I. INTRODUCTION

PWM DC-DC power converters are widely used in regulated DC power supplies, DC motor drives, and battery chargers [1]-[7]. The input to a power converter is usually an unregulated DC voltage, obtained by rectifying the AC line voltage, which has a large voltage variations due to changes in the line voltage magnitude. PWM DC-DC converters are used to convert the unregulated DC input into a controlled DC output at a desired voltage level. The purpose of this paper is threefold. First, a new non-symmetric phase controller is introduced, which provides a peak phase boost of up to 165° with its phase returning to 0° at high frequencies. Secondly, open and closed-loop characteristics of a boost PWM converter with the new controller are given. Finally, Euler's identity is utilized to express the closed-loop small-signal characteristic transfer functions in terms of defined converter magnitudes and phases. This format is conducive to modeling in any high level programming language such as the data analysis software package Axum 3.0 by TriMetrix Inc. which combines a programming language, spreadsheet, and publication quality technical graphics.

II. BOOST POWER STAGE

The PWM boost converter, Fig. 1, consists of a power MOSFET as a switch S , a diode $D1$, an inductor L , a filter capacitor C , and a load resistance R . The converter takes a DC input voltage V_I and increases it to a desired output voltage V_O seen across the load R . The power stage design specification to be used through the remainder of the paper to illustrate the closed-loop converter design is: CCM operation, $V_I = 12 \pm 2$ V, $V_O = 20$ V, $I_O = 0.3 \pm 0.2$ A, $f_s = 100$ kHz, and $V_r/V_O \leq 1\%$; where V_r is the maximum peak-to-peak voltage ripple on the DC output voltage. Using component design equations [7], the following component values were chosen to meet the design specifications. The load resistance $R = V_O/I_O$ has a range of $R_{min} = 40 \Omega$ to $R_{max} = 200 \Omega$. The DC voltage gain $M_{V_{DC}} = V_O/V_I$

has a range of $M_{V_{DCmin}} = 1.43$ to $M_{V_{DCmax}} = 2.00$, with a nominal value of $M_{V_{DCnom}} = 1.67$. Assuming a converter efficiency of 85%, the corresponding range of duty ratio $D = 1 - \eta/M_{V_{DC}}$ required to maintain the DC voltage gain is $D_{max} = 0.575$ to $D_{min} = 0.406$, with a nominal duty ratio of $D_{nom} = 0.509$. To ensure CCM operation for the boost converter for the range of duty ratio, the inductor was made using a Philips ferrite pot core 2616 PA A00 3C8 and 25.5 turns of Belden solid copper magnet wire with AWG 24. The measured inductance was $L = 156 \mu\text{H}$ and the measured ESR of the inductor was $r_L = 0.19 \Omega$ at DC. To ensure the output voltage ripple is less than 1% of the output voltage, a 68 μF metal film capacitor is chosen which has a measured ESR of $r_C = 0.111 \Omega$ at $f = 100$ kHz. The switching components chosen were an International Rectifier power MOSFET IRF 530 (100V/14A) with the ON-resistance $r_{DS} = 0.18 \Omega$ and a Motorola ultrafast power diode MUR 410 (100V/4A) with a forward resistance of $R_F = 0.160 \Omega$ and an offset voltage of $V_F = 0.65$ V.

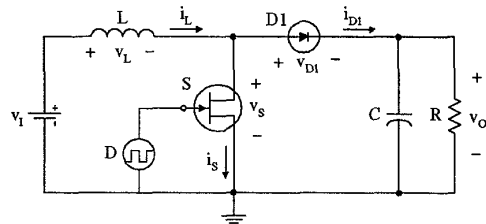


Fig. 1: Boost converter power stage.

III. SMALL-SIGNAL CHARACTERISTICS

The power stage is modeled by a linear circuit [1] which linearizes the nonlinear switching components of the power stage as shown in Fig. 2. The two switching components are replaced by dependent voltage and current sources which describe the average operation of the power stage switching network. By the principle of superposition, the linear circuit model can be separated into a DC model and a small-signal model [1]. The small-signal model of the power stage is obtained from the linear circuit model by replacing the DC voltage sources V_I and $(1-D)V_O$ with short circuits, and replacing the DC current source $(1-D)I_L$ with an open circuit. Likewise, the small-signal model of the controller is obtained by replacing the DC voltage source V_R with a short circuit. Parasitic components of the power stage include ESR of the capacitor r_C , ESR of the inductor r_L , MOSFET ON-resistance r_{DS} , and diode forward resistance R_F and threshold voltage V_F . The equivalent series resistance r consists of the inductor ESR r_L plus the equivalent averaged resistances seen in each of the two switching branches, MOSFET and diode, reflected onto the inductor branch. This resistance is given by [1]

$$(1) \quad r = r_L + D r_{DS} + (1-D) R_F + D(1-D) \frac{r_C R}{r_C + R}$$

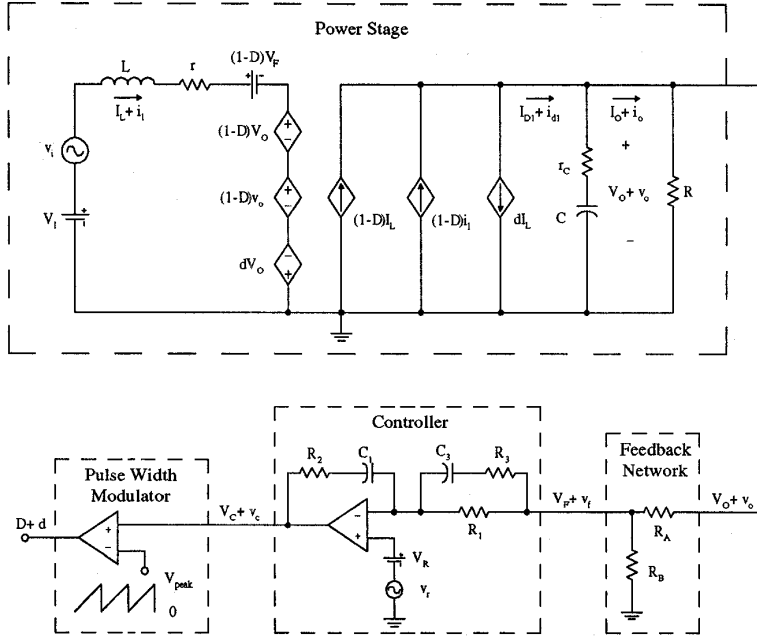


Fig. 2: Linear circuit model of the PWM boost DC-DC converter with a non-symmetric phase control circuit.

and has a value of $r = 0.388 \Omega$ at a nominal duty ratio $D = 0.5$. Power stage and closed-loop small-signal transfer functions are derived for control-to-output, input-to-output, input and output impedances [7].

A. Pulse-Width-Modulator

The pulse-width-modulator of Fig. 2 is a non-inverting comparator and employs a fixed frequency, fixed amplitude sawtooth waveform for comparison with a changing control voltage to generate the duty ratio drive signal to the MOSFET. The period of the sawtooth waveform establishes the MOSFET switching frequency f_s . With a peak sawtooth voltage of $V_{peak} = 0.7 \text{ V}$, the transfer function of the pulse-width-modulator [3], [4], [5] is given as the inverse peak sawtooth voltage

$$(2) \quad T_m(s) \equiv \frac{d(s)}{v_c(s)} = \frac{1}{V_{peak}} = 0.200 = -13.98 \text{ dB}.$$

B. Feedback Network

The feedback network [8] of Fig. 2 steps down the boost converter output voltage to the reference voltage level, where reference voltage $V_R = 2.5 \text{ V}$ corresponds to a nominal duty ratio of $D_{nom} = 0.509$. The transfer function of the feedback network [5] is given by

$$(3) \quad T_b(s) \equiv \frac{v_f(s)}{v_o(s)} = \frac{V_R}{V_O} = \frac{R_B}{R_A + R_B} = 0.125 = -17.99 \text{ dB}.$$

Choosing resistor $R_B = 620 \Omega$, then resistor $R_A = 4.3 \text{ k}\Omega$.

C. Power Stage and Plant Control-to-Output Transfer Function

The power stage control-to-output transfer function is derived from Fig. 2 in the small-signal model configuration with the AC input voltage reduced to zero. Using this model, the transfer function is derived as

$$(4) \quad T_p(s) \equiv \frac{v_o(s)}{d(s)} \Big|_{v_i(s)=0} = \frac{-V_O r_c}{(R + r_c)(1-D)} \cdot \frac{(s + \omega_{zn})(s - \omega_{zp})}{s^2 + 2\xi\omega_o s + \omega_o^2}.$$

The angular frequency of the left-half plane (LHP) zero is given by

$$(5) \quad \omega_{zn} = \frac{1}{Cr_c},$$

and has a value of $f_{zn} = 21.086 \text{ kHz}$ for component values given in the design example. The angular frequency of the right-half plane (RHP) zero is given by

$$(6) \quad \omega_{zp} = \frac{1}{L}[(1-D)^2 R - r],$$

which has a value $f_{zp} = 9.806 \text{ kHz}$ at a nominal duty ratio of $D = 0.5$ and load $R = R_{min}$. The natural undamped frequency and damping ratio are given by

$$(7) \quad \omega_o = \sqrt{\frac{r + R(1-D)^2}{LC(R + r_c)}} \quad \text{and} \quad \xi = \frac{C[r(R + r_c) + Rr_c(1-D)^2] + L}{2\sqrt{LC(R + r_c)[r + R(1-D)^2]}}$$

respectively, and have values of $f_o = 786 \text{ Hz}$ and $\xi = 0.307$ at a nominal duty ratio $D = 0.5$ and load $R = R_{min}$.

The transfer function characteristics of all elements in the open-loop, excluding the controller, must be defined prior to designing the controller. The pulse-width modulator and power stage define the plant and when combined with the feedback network provide a control-to-output transfer function $T_2(s) \equiv T_m T_b T_p(s)$ given as

$$(8) \quad T_2(s) \equiv \frac{v_f(s)}{v_c(s)} = \frac{1}{V_{peak}} \cdot \frac{R_B}{R_A + R_B} \cdot \frac{-V_O r_c}{(R + r_c)(1-D)} \cdot \frac{(s + \omega_{zn})(s - \omega_{zp})}{s^2 + 2\xi\omega_o s + \omega_o^2}.$$

From this transfer function, the magnitude and phase can easily be obtained and are illustrated as Bode plots in Fig. 3(a) and (b) respectively, for a duty ratio of 0.4, 0.5, and 0.6.

D. Controller

The converter requires a controller for the following reasons: to reduce DC error, output impedance, line noise, and sensitivity of the closed-loop gain to component values over a wide frequency range, and to

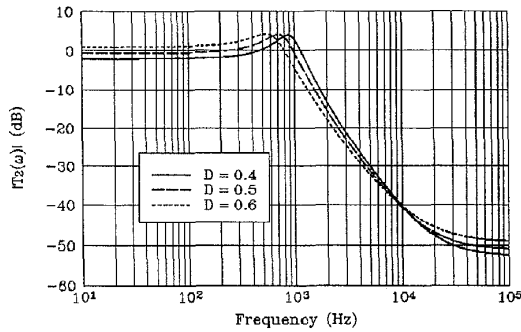
satisfy the sufficient conditions of relative stability: a gain margin (GM) of 6 to 12 dB and a phase margin (PM) of 45° to 60°. The small-signal voltage transfer function of the controller of Fig. 2 is

$$(9) \quad T_c(s) \equiv \frac{v_c(s)}{v_e(s)} = \frac{v_c(s)}{v_r(s) - v_f(s)} \Big|_{v_r=0} = -\frac{v_c(s)}{v_f(s)} = -A_v(s) = \frac{Z_2}{Z_1},$$

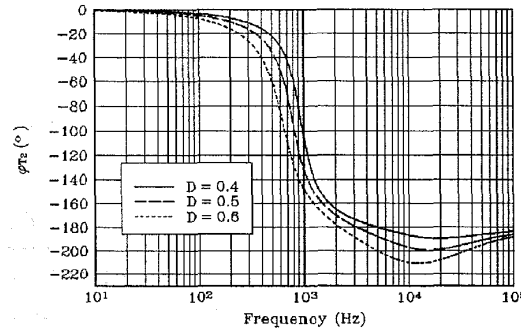
where

$$(10) \quad Z_1 = \frac{\Re}{R_1 + R_3} \cdot \frac{s + \frac{R_1 + R_\beta}{C_3 \Re}}{s + \frac{1}{C_3(R_1 + R_3)}} \quad \text{and} \quad Z_2 = \frac{R_2}{s} \left(s + \frac{1}{R_2 C_1} \right),$$

where $\Re = R_1 R_3 + R_\beta(R_1 + R_3)$ and the loading effect of the feedback network on the controller is $R_\beta = R_A \parallel R_B$.



(a)



(b)

Fig. 3: Plant T_2 and feedback network control-to-output transfer function. (a) Magnitude vs. frequency. (b) Phase vs. frequency.

The controller transfer function is expressed using (9) and (10) as

$$(11) \quad T_c(s) = \frac{R_2(R_1 + R_3)}{R_1 R_3 + R_\beta(R_1 + R_3)} \cdot \frac{(s + \omega_{zc1})(s + \omega_{zc2})}{s(s + \omega_{pc})},$$

where

$$(12) \quad \omega_{zc1} = \frac{1}{C_1 R_2}, \quad \omega_{zc2} = \frac{1}{C_3(R_1 + R_3)},$$

and

$$(13) \quad \omega_{pc} = \frac{R_1 + R_\beta}{C_3[R_1 R_3 + R_\beta(R_1 + R_3)]}.$$

Designing the controller such that $\omega_{zc1} = \omega_{zc2} = \omega_{zc}$ allows a K -factor [9] to be defined as

$$(14) \quad K = \frac{\omega_{pc}}{\omega_{zc1}} = \frac{\omega_{pc}}{\omega_{zc2}} = \frac{C_1 R_2(R_1 + R_\beta)}{C_3[R_1 R_3 + R_\beta(R_1 + R_3)]} = \frac{(R_1 + R_3)(R_1 + R_\beta)}{R_1 R_3 + R_\beta(R_1 + R_3)}.$$

The transfer function can be rewritten using (14) and letting $s = j\omega$ as

$$(15) \quad T_c(j\omega) = \frac{R_2(R_1 + R_3)}{R_1 R_3 + R_\beta(R_1 + R_3)} \cdot \frac{\omega_{zc}}{K} \cdot \frac{\left(1 + \frac{j\omega}{\omega_{zc}}\right)^2}{j\omega \left(1 + \frac{j\omega}{\omega_{pc}}\right)},$$

from which the phase may be expressed as

$$(16) \quad \phi_{T_c}(\omega) = -\frac{\pi}{2} + \arctan \left[\frac{\frac{2\omega}{\omega_{zc}} - \frac{\omega}{\omega_{pc}} + \left(\frac{\omega}{\omega_{pc}}\right)\left(\frac{\omega}{\omega_{zc}}\right)^2}{1 + \left(\frac{2\omega}{\omega_{zc}}\right)\left(\frac{\omega}{\omega_{pc}}\right) - \left(\frac{\omega}{\omega_{zc}}\right)^2} \right].$$

For a symmetric phase controller [9], where the coincident number of zeros are equal to the coincident number of poles in addition to the pole at the origin, the maximum value of phase ϕ_{T_c} occurs at the geometric mean of the zero frequency and the pole frequency. Since the controller under design has two coincident zeros $\omega_{zc1} = \omega_{zc2} = \omega_{zc}$ and only one pole ω_{pc} , the maximum value of phase ϕ_{T_c} is offset from the geometric mean of the zero and pole frequencies. In designing multiple variations of this controller without a defined design procedure, it was noticed that the maximum controller phase frequency f_m always occurred at a fixed offset from the geometric mean of the controller pole frequency ω_{pc} and zero frequency ω_{zc} . This peak phase offset constant

$N_{rg} = f_m / \sqrt{f_{pc} f_{zc}}$ was found to be $N_{rg} = 2.25$. The peak phase offset constant allows the application of the K -factor design approach to the non-symmetric phase controller. The maximum value of phase ϕ_{T_c} for the non-symmetric controller occurs at frequency ω_m and is equal to the 0-dB crossover frequency ω_c of the control-to-output transfer function of the plant $T_2(\omega)$. The frequency at peak phase is given by

$$(17) \quad \omega_m = \omega_c = \sqrt{N_{rg} \omega_{zc} \omega_{pc}},$$

which is rewritten in terms of the K -factor expression using (14) as

$$(18) \quad \omega_m = \omega_c = \sqrt{N_{rg} K \omega_{zc}^2} = \omega_{zc} \sqrt{N_{rg} K} = \sqrt{\frac{N_{rg} \omega_{pc}^2}{K}} = \omega_{pc} \sqrt{\frac{N_{rg}}{K}}.$$

The controller magnitude $|T_c|$ at the peak controller phase frequency ω_m is found by combining (12), (14), (15), and (18) as

$$(19) \quad |T_c(\omega_m)| = \frac{1}{\omega_m C_1 (R_1 + R_\beta)} \cdot \frac{1 + N_{rg} K}{\sqrt{1 + \frac{N_{rg}}{K}}}.$$

Converting from radian to hertz and noting that the crossover frequency f_c is equal to the controller peak phase frequency f_m , the magnitude of the controller is expressed as

$$(20) \quad |T_c(f_c)| = |T_c(f_m)| = \frac{1}{2\pi f_c C_1 (R_1 + R_\beta)} \cdot \frac{1 + N_{rg} K}{\sqrt{1 + \frac{N_{rg}}{K}}}$$

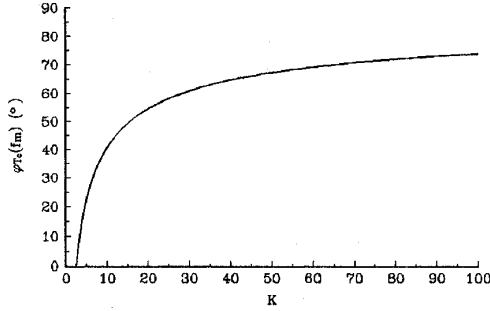


Fig. 4: Peak controller phase vs. K -factor.

The peak controller phase is found by combining (16) and (18) as

$$(21) \quad \varphi_{T_c}(f_m) = -90^\circ + \arctan \left[\frac{\sqrt{N_{rg}}(2K - 1 + KN_{rg})}{\sqrt{K}(2N_{rg} + 1 - KN_{rg})} \right],$$

from which the peak controller phase as a function of the K -factor may be plotted as shown in Fig. 4. Observe that the peak phase boost of the controller $\varphi_{T_c}(f_m)$ increases from zero to 75° as K is increased from nearly zero to 100. The magnitude of the open-loop gain at the crossover frequency $f_c = f_m$ is

$$(22) \quad |T_{pol}(f_c)| = |T_c(f_c)| \cdot |T_2(f_c)| = 1.$$

The open-loop phase shift at the crossover frequency $f_c = f_m$ is

$$(23) \quad \varphi_{T_{pol}}(f_c) = \varphi_{T_2}(f_c) + \varphi_{T_c}(f_c).$$

The phase margin (PM) is obtained as

$$(24) \quad PM = 180^\circ + \varphi_{T_{pol}}(f_c) = 180^\circ + \varphi_{T_2}(f_c) + \varphi_{T_c}(f_c),$$

and it follows that the required peak controller phase boost is given by

$$(25) \quad \varphi_{T_c}(f_c) = PM - \varphi_{T_2}(f_c) - 180^\circ.$$

E. Controller Design Procedure

Pick the desired crossover frequency from transfer function $T_2(s)$ at a frequency close to where the phase first crosses -180° , which occurs at $f_c = 2$ kHz from Fig. 3(b). At this frequency and for the worst case duty ratio $D = 0.6$, the magnitude of the plant is $|T_2(f_c)| = -17.85$ dB = 0.128 and the phase of the plant is $\varphi_{T_2}(f_c) = -177.91^\circ$. Assuming a phase margin of $PM = 60^\circ$, the required controller phase boost is obtained from (25) as

$$(26) \quad \varphi_{T_c}(f_c) = 60^\circ - (-177.91^\circ) - 180^\circ = 57.91^\circ.$$

Using Fig. 4, the K -factor for a peak controller phase of 57.91° is $K = 25$. The loading resistance upon the controller, due to the feedback network is calculated as

$$(27) \quad R_\beta = R_A \parallel R_B = \frac{R_A R_B}{R_A + R_B} = 542 \, \Omega.$$

Assuming $R_1 = 100$ k Ω , resistance R_3 may be calculated from (14) as

$$(28) \quad R_3 = \frac{R_1(R_1 + R_\beta) - KR_1 R_\beta}{(R_1 + R_\beta)(K - 1)} = 3.605 \, \text{k}\Omega.$$

Pick a standard resistor $R_3 = 3.6$ k Ω . Capacitor C_1 may be derived from (20) and (22) as

$$(29) \quad C_1 = \frac{1}{(2\pi f_c)(R_1 + R_\beta)} \cdot \frac{1 + N_{rg} K}{\sqrt{1 + \frac{N_{rg}}{K}}} |T_2(f_c)| = 5.56 \, \text{nF}.$$

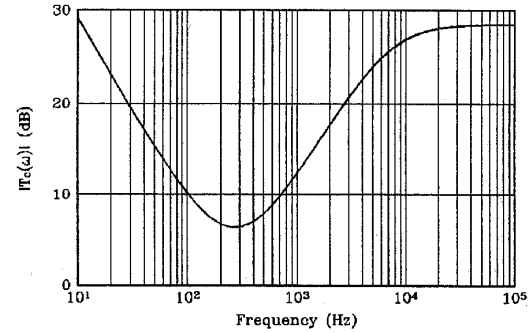
A Panasonic[®] polypropylene capacitor was chosen as $C_1 = 5.6$ nF. Resistor R_2 may be calculated from (12) and (18) as

$$(30) \quad R_2 = \frac{1}{2\pi f_c C_1} \sqrt{N_{rg} K} = 106.58 \, \text{k}\Omega.$$

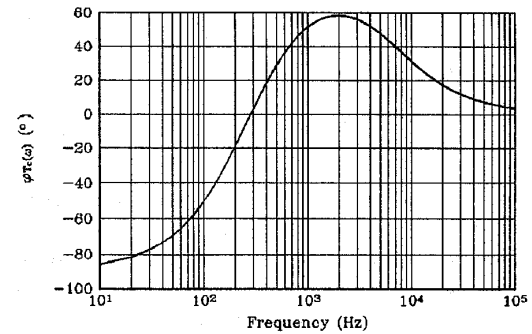
Pick a standard resistor $R_2 = 107$ k Ω . Capacitor C_3 may be calculated from (14) as

$$(31) \quad C_3 = \frac{C_1 R_2}{R_1 + R_3} = 5.783 \, \text{nF}.$$

A Panasonic[®] polypropylene capacitor was chosen as $C_3 = 5.6$ nF.



(a)



(b)

Fig. 5: Controller transfer function, T_c . (a) Magnitude vs. frequency. (b) Phase vs. frequency.

Using (11) and the above derived component values, the controller magnitude and phase are illustrated as Bode plots in Fig. 5(a) and (b), respectively. The controller pole and zero frequencies are calculated

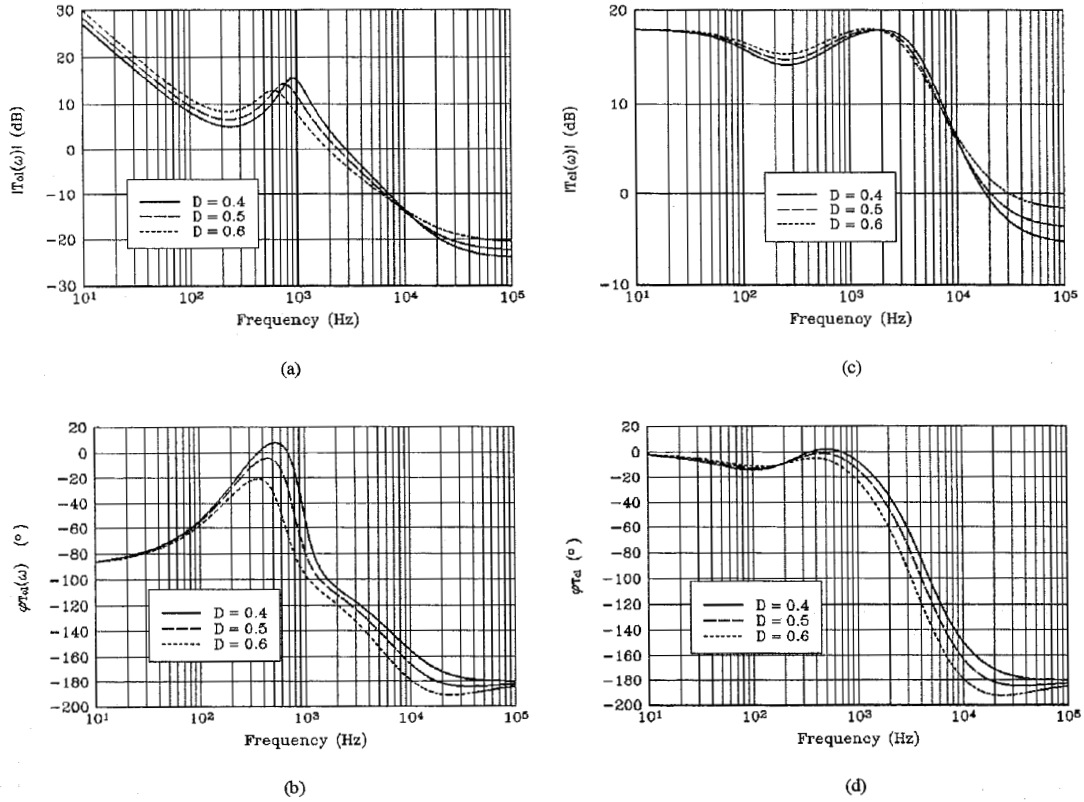


Fig. 6: Open-loop T_{pol} and closed-loop T_{pcl} control-to-output transfer functions. (a) Open-loop magnitude vs. frequency. (b) Open-loop phase vs. frequency. (c) Closed-loop magnitude vs. frequency. (d) Closed-loop phase vs. frequency.

using standard resistor and capacitor values from (12) and (13) as $f_{zc1} = 265$ Hz, $f_{zc2} = 275$ Hz and $f_{pc} = 6.866$ kHz. The peak controller phase frequency f_m is calculated from (17) as $f_m = 2.023$ kHz, which is close to the chosen crossover frequency. The difference between the chosen crossover frequency and the peak controller frequency is the result of using standard component values instead of theoretical.

F. Open and Closed-Loop Control-to-Output Transfer Functions

The open-loop transfer function of the boost converter is found from Fig. 2 as

$$(32) \quad T_{pol}(s) \equiv \frac{v_f(s)}{v_e(s)} \Big|_{v_i=0} = T_c(s)T_2(s).$$

The open-loop magnitude and phase are found from (32) and illustrated as Bode plots in Fig. 6(a) and (b), respectively, for three values of D . From the open-loop transfer functions of Fig. 6(a) and (b), the converter's phase margin (PM) may be found as 63.4°, 63.2° and 61.2°, and gain margin (GM) may be found as 23.9 dB, 18.18 dB and 13.77 dB, for duty ratios of 0.4, 0.5 and 0.6, respectively.

The closed-loop control-to-output transfer function is derived from Fig. 2 in the small-signal configuration with the AC input voltage reduced to zero. Using this model, the closed-loop transfer function is derived as

$$(33) \quad T_{pcl}(s) \equiv \frac{v_o(s)}{v_r(s)} \Big|_{v_i(s)=0} = \frac{T_c T_m T_p(s)}{1 + T_b T_c T_m T_p(s)} = \frac{1}{T_b} \cdot \frac{T_{pol}(s)}{1 + T_{pol}(s)}.$$

Letting $s = j\omega$ and expressing the transfer function in terms of magnitude and phase results in

$$(34) \quad |T_{pcl}| e^{j\varphi_{T_{pcl}}} = \frac{1}{T_b} \cdot \frac{|T_{pol}| e^{j\varphi_{T_{pol}}}}{1 + |T_{pol}| e^{j\varphi_{T_{pol}}}},$$

which is factored using Euler's identity, $e^{\pm j\theta} = \cos \theta \pm j \sin \theta$, as

$$(35) \quad |T_{pcl}| e^{j\varphi_{T_{pcl}}} = \frac{|T_{pol}| \left[(\cos \varphi_{T_{pol}} + |T_{pol}|) + j \sin \varphi_{T_{pol}} \right]}{|T_b| \left[|T_{pol}|^2 + 2|T_{pol}| \cos \varphi_{T_{pol}} + 1 \right]}.$$

The closed-loop magnitude of the control-to-output transfer function can be expressed as

$$(36) \quad |T_{pcl}| = \frac{|T_{pol}|}{|T_b| \sqrt{|T_{pol}|^2 + 2|T_{pol}| \cos \varphi_{T_{pol}} + 1}},$$

and the phase as

$$(37) \quad \varphi_{T_{pcl}} = \arctan \left(\frac{\sin \varphi_{T_{pol}}}{\cos \varphi_{T_{pol}} + |T_{pol}|} \right).$$

Transfer function magnitude and phase are illustrated as Bode plots in Fig. 6(c) and (d), respectively, for three values of D . From the closed-loop magnitude transfer function of Fig. 6(c), the converter's 3-dB

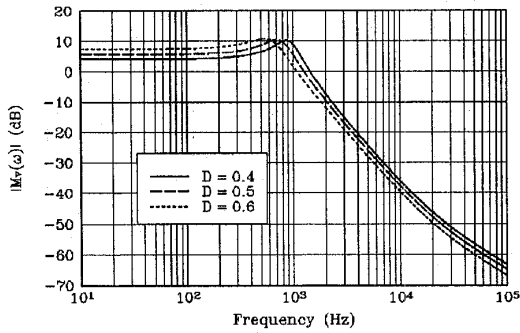
bandwidth (BW) may be found as 4.625 kHz, 4.190 kHz and 3.880 kHz for duty ratios of 0.4, 0.5 and 0.6, respectively.

G. Power Stage and Closed-Loop Input-to-Output Transfer Function

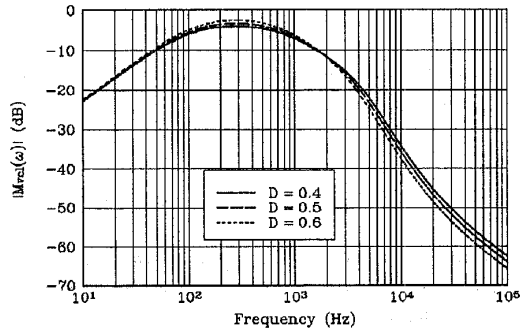
The input-to-output voltage transfer function of the power stage is derived from Fig. 2 in the small-signal model configuration with the AC duty ratio reduced to zero. Using this model, the input-to-output voltage transfer function is derived as

$$(38) \quad M_v(s) \equiv \frac{v_o(s)}{v_i(s)} \bigg|_{d(s)=0} = \frac{(1-D)Rr_c}{L(R+r_c)} \cdot \frac{s + \omega_{zn}}{s^2 + 2\xi\omega_o s + \omega_o^2},$$

where the frequency of the LHP zero ω_{zn} , the natural undamped frequency ω_o , and the damping ratio ξ are defined by (5) and (7), respectively.



(a)



(b)

Fig. 7: Power Stage M_v and closed-loop M_{vcl} input-to-output voltage transfer functions. (a) Power stage magnitude vs. frequency. (b) Closed-loop magnitude vs. frequency.

The closed-loop input-to-output voltage transfer function is derived from Fig. 2 in the small-signal model configuration with the AC reference voltage reduced to zero. Using this model, the input-to-output voltage transfer function is derived as

$$(39) \quad M_{vcl}(s) \equiv \frac{v_o(s)}{v_i(s)} \bigg|_{v_r(s)=0} = \frac{M_v(s)}{1 + T_b T_c T_m T_p(s)} = \frac{M_v(s)}{1 + T_{ol}(s)},$$

Expressing the transfer functions in terms of the magnitude and phase and applying Euler's identity, the closed-loop magnitude of the input-to-output voltage transfer function is expressed as

$$(40) \quad |M_{vcl}| = \frac{|M_v|}{\sqrt{|T_{pol}|^2 + 2|T_{pol}|\cos\phi_{T_{pol}} + 1}}.$$

The power stage magnitude derived from (38) and the closed-loop magnitude are illustrated as Bode plots in Fig. 7(a) and (b), respectively, for three values of D .

H. Power Stage and Closed-Loop Input Impedance

The input impedance of the power stage is derived from Fig. 2 in the small-signal model configuration with the AC duty ratio reduced to zero. Using this model, the input impedance is derived as

$$(41) \quad Z_i(s) \equiv \frac{v_i(s)}{i_i(s)} \bigg|_{d(s)=0} = L \cdot \frac{s^2 + 2\xi\omega_o s + \omega_o^2}{s + \omega_{rc}},$$

where the angular frequency of the LHP pole is

$$(42) \quad \omega_{rc} = \frac{1}{C(R+r_c)},$$

which has a value $f_{rc} = 58$ Hz at a load $R = R_{min}$. The natural undamped frequency ω_o and damping ratio ξ are defined by (7).

The closed-loop input impedance is derived from Fig. 2 in the small-signal model configuration with the AC reference voltage reduced to zero. Using this model, the input impedance is derived as

$$(43) \quad Z_{icl}(s) \equiv \frac{v_i(s)}{i_i(s)} \bigg|_{v_r(s)=0} = \frac{Z(s)}{M_{vcl}(s)} \left[\frac{(1-D)^2}{(1-D) - I_O T_b T_m T_c(s) Z(s)} \right],$$

where the impedance of the power stage output RC filter is defined as

$$(44) \quad Z(s) = \frac{Rr_c}{R+r_c} \cdot \frac{s + \omega_{zn}}{s + \omega_{rc}}.$$

The zero frequency ω_{zn} and pole frequency ω_{rc} are defined by (5) and (42), respectively. Expressing the input impedance in terms of the magnitude and phase of previously defined transfer functions and applying Euler's identity, the closed-loop input impedance magnitude is expressed as

$$(45) \quad |Z_{icl}| = \frac{(1-D)^2 |Z| \sqrt{|T_{pol}|^2 + 2|T_{pol}|\cos\phi_{T_{pol}} + 1}}{|M_v| \sqrt{A^2 + B^2}},$$

where

$$(46) \quad A = (1-D)\cos\phi_Z - I_O T_b T_m |T_c| |Z| \cos\phi_{T_c}$$

and

$$(47) \quad B = (D-1)\sin\phi_Z - I_O T_b T_m |T_c| |Z| \sin\phi_{T_c}.$$

The input impedance of the power stage derived from (41), and of the closed-loop converter are illustrated as Bode plots in Fig. 8(a) and (b), respectively, for three values of D . Further factoring of (43) allows us to express the real closed-loop input impedance component as

$$(48) \quad R_{icl} = \frac{(1-D)^2 |Z|}{|M_{vcl}| (A^2 + B^2)} \cdot (A \cos\phi_{M_{vcl}} - B \sin\phi_{M_{vcl}})$$

and the imaginary closed-loop input impedance component as

$$(49) \quad X_{icl} = \frac{(1-D)^2 |Z|}{|M_{vcl}| (A^2 + B^2)} \cdot (A \sin\phi_{M_{vcl}} + B \cos\phi_{M_{vcl}}).$$

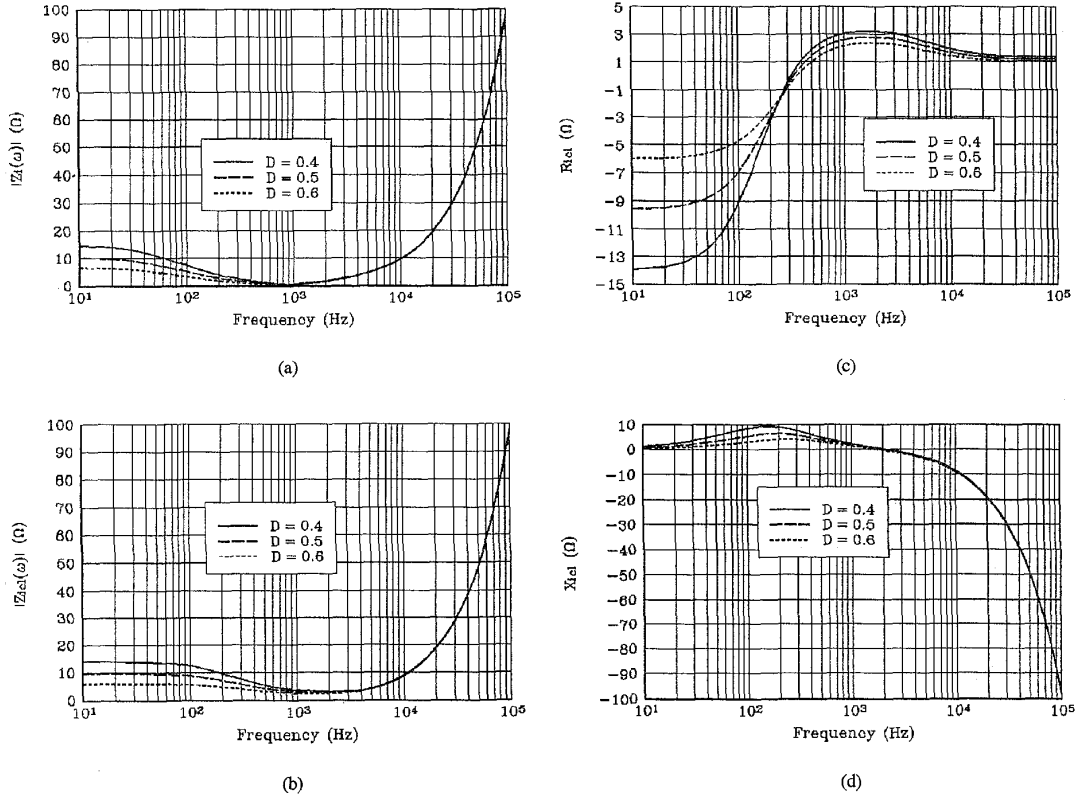


Fig. 8: Power stage Z_i , closed-loop Z_{icl} , and closed-loop complex R_{icl} and X_{icl} input impedance transfer functions. (a) Power stage magnitude vs. frequency. (b) Closed-loop magnitude vs. frequency. (c) Closed-loop real impedance component vs. frequency. (d) Closed-loop imaginary impedance component vs. frequency.

The real and imaginary components of the closed-loop converter input impedance are modeled in Fig. 8(c) and (d) respectively, for three values of D . The presence of negative resistance, a potential source of instability, is evident in the real component of the closed-loop input impedance of Fig. 8(c). All closed-loop DC-DC converters experience negative resistance at DC and low frequencies to maintain a constant output voltage, $P_I = V_I I_I = V_O I_O = P_O = \text{constant}$. When V_I increases a counter effect occurs where I_I decreases, resulting in negative resistance.

I. Power Stage and Closed-Loop Output Impedance

The output impedance of the power stage is derived from Fig. 2 in the small-signal model configuration with the AC duty ratio and the AC input voltage reduced to zero. Using this model, the output impedance is

$$(50) \quad Z_o(s) \equiv \frac{v_o(s)}{i_o(s)} \bigg|_{\substack{d(s)=0 \\ v_i(s)=0}} = \frac{R r_C}{R + r_C} \cdot \frac{(s + \omega_{zn})(s + \omega_{ol})}{s^2 + 2\xi\omega_o s + \omega_o^2},$$

where the frequency of one of the LHP poles is

$$(51) \quad \omega_{ol} = \frac{r}{L},$$

and has a value of $f_{ol} = 396$ Hz. The frequency of the LHP pole ω_{zn} , the natural undamped frequency ω_o , and the damping constant ξ are defined by (5) and (7), respectively.

The closed-loop output impedance of the converter is derived from Fig. 2 in the small-signal model configuration with the AC input and AC reference voltages reduced to zero, and a test current $i_t(s)$ injected into the load of the power stage. The injected current produces a test voltage

$v_t(s)$ due to the closed-loop output impedance. Using this model, the input impedance is derived as

$$(52) \quad Z_{ocl}(s) \equiv \frac{v_t(s)}{i_t(s)} \bigg|_{\substack{v_i(s)=0 \\ v_r(s)=0}} = \frac{Z_o(s)}{1 + T_b T_c T_m T_p(s)} = \frac{Z_o(s)}{1 + T_{pol}(s)}.$$

Expressing the output impedance transfer functions in terms of the magnitude and phase and applying Euler's identity, the closed-loop output impedance magnitude is expressed as

$$(53) \quad |Z_{ocl}| = \frac{|Z_o|}{\sqrt{|T_{pol}|^2 + 2|T_{pol}|\cos\phi_{T_{pol}} + 1}}.$$

The power stage magnitude derived from (50), and closed-loop magnitude are illustrated as Bode plots in Fig. 9(a) and (b) respectively, for three values of D . Further factoring of (52) allows us to express the real closed-loop input impedance component as

$$(54) \quad R_{ocl} = \frac{|Z_o| \cdot (\cos\phi_{Z_o} + |T_{pol}|\cos(\phi_{T_{pol}} - \phi_{Z_o}))}{1 + 2|T_{pol}|\cos\phi_{T_{pol}} + |T_{pol}|^2}$$

and the imaginary closed-loop input impedance component as

$$(55) \quad X_{ocl} = \frac{|Z_o| \cdot (\sin\phi_{Z_o} - |T_{pol}|\sin(\phi_{T_{pol}} - \phi_{Z_o}))}{1 + 2|T_{pol}|\cos\phi_{T_{pol}} + |T_{pol}|^2}.$$

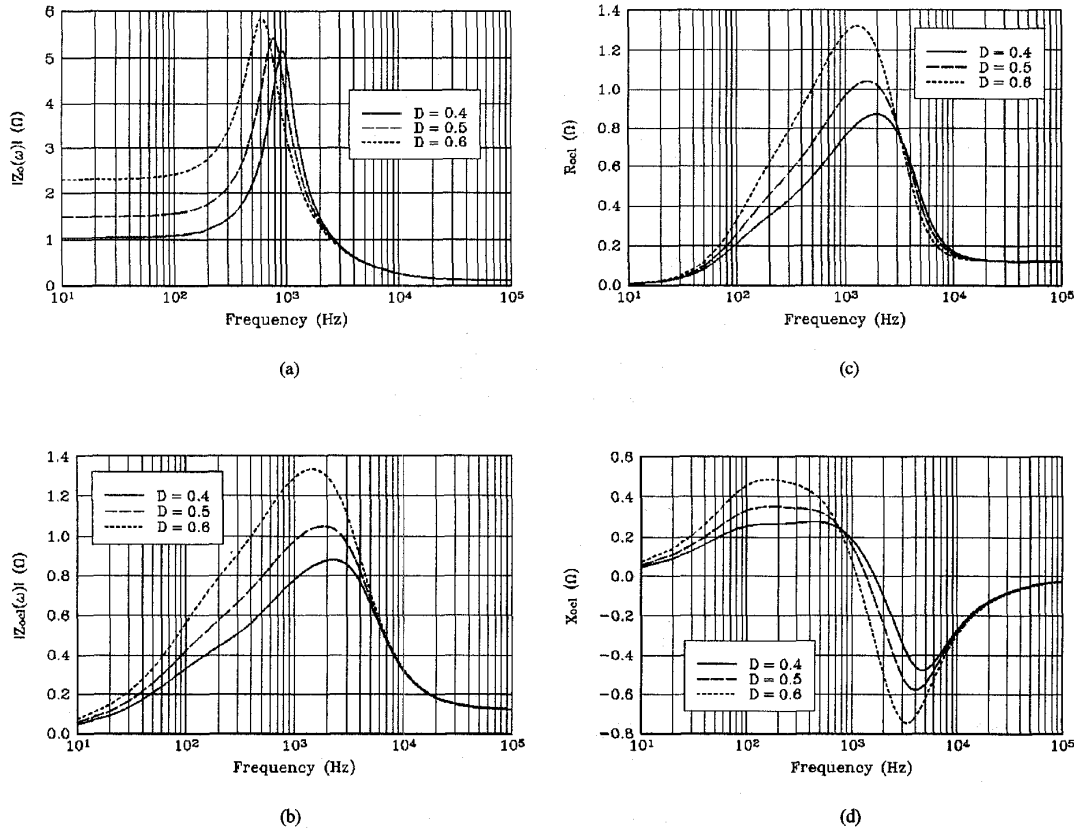


Fig. 9: Power stage Z_o , closed-loop Z_{oel} , and closed-loop complex R_{oel} and X_{oel} output impedance transfer functions. (a) Power stage magnitude vs. frequency. (b) Closed-loop magnitude vs. frequency. (c) Closed-loop real impedance component vs. frequency. (d) Closed-loop imaginary impedance component vs. frequency.

The real and imaginary components of the closed-loop output impedance are modeled in Fig. 9(c) and (d), respectively, for three values of D . As expected for a constant DC output voltage converter, the real component of the closed-loop output impedance is positive for all frequencies.

IV. CONCLUSIONS

Open and closed-loop transfer functions for a voltage-mode control strategy for a PWM boost DC-DC converter have been derived and illustrated. A design procedure was introduced for a new non-symmetric phase controller using a K -factor approach [9], previously defined for controllers with symmetric phase distribution. The closed-loop transfer functions have been derived solely in terms of defined converter magnitude and phase components, which allows modeling in any high level programming language. The converters open and closed-loop control-to-output transfer function characteristics include an 13.77 dB to 23.9 dB gain margin, a phase margin of 61.2° to 63.4°, and a 3-dB BW of 3.880 kHz to 4.625 kHz. The new controller's peak phase boost of up to 165°, with its phase returning to 0° at high frequencies compensates for the -90° of phase due to the RHP zero ω_{zn} inherent in the boost converter. The phase of the non-symmetric phase controller is much improved over that of a commonly used symmetric phase integral-lead controller, which provides -90° of phase at high frequencies. The new controllers characteristics provide increased gain margin and phase margin and improved stability to a DC-DC converter.

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